Place and route

Release 14.7 par P.20131013 (nt64)

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DESKTOP-NRV290J:: Sun Jul 10 19:49:38 2022

par -w -intstyle ise -ol high -mt off WS\_map.ncd WS.ncd WS.pcf

Constraints file: WS.pcf.

Loading device for application Rf\_Device from file '7a100t.nph' in environment C:\Xilinx\14.7\ISE\_DS\ISE\.

"WS" is an NCD, version 3.2, device xa7a100t, package csg324, speed -2i

Initializing temperature to 100.000 Celsius. (default - Range: -40.000 to 100.000 Celsius)

Initializing voltage to 0.950 Volts. (default - Range: 0.950 to 1.050 Volts)

INFO:Par:282 - No user timing constraints were detected or you have set the option to ignore timing constraints ("par

-x"). Place and Route will run in "Performance Evaluation Mode" to automatically improve the performance of all

internal clocks in this design. Because there are not defined timing requirements, a timing score will not be

reported in the PAR report in this mode. The PAR timing summary will list the performance achieved for each clock.

Note: For the fastest runtime, set the effort level to "std". For best performance, set the effort level to "high".

Device speed data version: "PRELIMINARY 1.07 2013-10-13".

Device Utilization Summary:

Slice Logic Utilization:

Number of Slice Registers: 1 out of 126,800 1%

Number used as Flip Flops: 0

Number used as Latches: 1

Number used as Latch-thrus: 0

Number used as AND/OR logics: 0

Number of Slice LUTs: 2 out of 63,400 1%

Number used as logic: 2 out of 63,400 1%

Number using O6 output only: 2

Number using O5 output only: 0

Number using O5 and O6: 0

Number used as ROM: 0

Number used as Memory: 0 out of 19,000 0%

Number used exclusively as route-thrus: 0

Slice Logic Distribution:

Number of occupied Slices: 1 out of 15,850 1%

Number of LUT Flip Flop pairs used: 2

Number with an unused Flip Flop: 1 out of 2 50%

Number with an unused LUT: 0 out of 2 0%

Number of fully used LUT-FF pairs: 1 out of 2 50%

Number of slice register sites lost

to control set restrictions: 0 out of 126,800 0%

A LUT Flip Flop pair for this architecture represents one LUT paired with

one Flip Flop within a slice. A control set is a unique combination of

clock, reset, set, and enable signals for a registered element.

The Slice Logic Distribution report is not meaningful if the design is

over-mapped for a non-slice resource or if Placement fails.

OVERMAPPING of BRAM resources should be ignored if the design is

over-mapped for a non-BRAM resource or if placement fails.

IO Utilization:

Number of bonded IOBs: 21 out of 210 10%

Specific Feature Utilization:

Number of RAMB36E1/FIFO36E1s: 0 out of 135 0%

Number of RAMB18E1/FIFO18E1s: 0 out of 270 0%

Number of BUFG/BUFGCTRLs: 1 out of 32 3%

Number used as BUFGs: 1

Number used as BUFGCTRLs: 0

Number of IDELAYE2/IDELAYE2\_FINEDELAYs: 0 out of 300 0%

Number of ILOGICE2/ILOGICE3/ISERDESE2s: 0 out of 300 0%

Number of ODELAYE2/ODELAYE2\_FINEDELAYs: 0

Number of OLOGICE2/OLOGICE3/OSERDESE2s: 0 out of 300 0%

Number of PHASER\_IN/PHASER\_IN\_PHYs: 0 out of 24 0%

Number of PHASER\_OUT/PHASER\_OUT\_PHYs: 0 out of 24 0%

Number of BSCANs: 0 out of 4 0%

Number of BUFHCEs: 0 out of 96 0%

Number of BUFRs: 0 out of 24 0%

Number of CAPTUREs: 0 out of 1 0%

Number of DNA\_PORTs: 0 out of 1 0%

Number of DSP48E1s: 0 out of 240 0%

Number of EFUSE\_USRs: 0 out of 1 0%

Number of FRAME\_ECCs: 0 out of 1 0%

Number of IBUFDS\_GTE2s: 0 out of 4 0%

Number of ICAPs: 0 out of 2 0%

Number of IDELAYCTRLs: 0 out of 6 0%

Number of IN\_FIFOs: 0 out of 24 0%

Number of MMCME2\_ADVs: 0 out of 6 0%

Number of OUT\_FIFOs: 0 out of 24 0%

Number of PCIE\_2\_1s: 0 out of 1 0%

Number of PHASER\_REFs: 0 out of 6 0%

Number of PHY\_CONTROLs: 0 out of 6 0%

Number of PLLE2\_ADVs: 0 out of 6 0%

Number of STARTUPs: 0 out of 1 0%

Number of XADCs: 0 out of 1 0%

Overall effort level (-ol): High

Router effort level (-rl): High

Starting initial Timing Analysis. REAL time: 9 secs

Finished initial Timing Analysis. REAL time: 9 secs

Starting Router

Phase 1 : 29 unrouted; REAL time: 10 secs

Phase 2 : 27 unrouted; REAL time: 10 secs

Phase 3 : 2 unrouted; REAL time: 10 secs

Phase 4 : 2 unrouted; (Par is working to improve performance) REAL time: 13 secs

Updating file: WS.ncd with current fully routed design.

Phase 5 : 0 unrouted; (Par is working to improve performance) REAL time: 13 secs

Phase 6 : 0 unrouted; (Par is working to improve performance) REAL time: 13 secs

Phase 7 : 0 unrouted; (Par is working to improve performance) REAL time: 13 secs

Phase 8 : 0 unrouted; (Par is working to improve performance) REAL time: 13 secs

Phase 9 : 0 unrouted; (Par is working to improve performance) REAL time: 13 secs

Total REAL time to Router completion: 13 secs

Total CPU time to Router completion: 13 secs

Partition Implementation Status

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No Partitions were found in this design.

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Generating "PAR" statistics.

INFO:Par:459 - The Clock Report is not displayed in the non timing-driven mode.

Timing Score: 0 (Setup: 0, Hold: 0)

Asterisk (\*) preceding a constraint indicates it was not met.

This may be due to a setup or hold violation.

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Constraint | Check | Worst Case | Best Case | Timing | Timing

| | Slack | Achievable | Errors | Score

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Autotimespec constraint for clock net clo | SETUP | N/A| 0.799ns| N/A| 0

ck\_BUFGP | HOLD | 0.235ns| | 0| 0

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All constraints were met.

INFO:Timing:2761 - N/A entries in the Constraints List may indicate that the

constraint is not analyzed due to the following: No paths covered by this

constraint; Other constraints intersect with this constraint; or This

constraint was disabled by a Path Tracing Control. Please run the Timespec

Interaction Report (TSI) via command line (trce tsi) or Timing Analyzer GUI.

Generating Pad Report.

All signals are completely routed.

Total REAL time to PAR completion: 13 secs

Total CPU time to PAR completion: 13 secs

Peak Memory Usage: 5029 MB

Placer: Placement generated during map.

Routing: Completed - No errors found.

Number of error messages: 0

Number of warning messages: 0

Number of info messages: 2

Writing design to file WS.ncd

PAR done!